Towards ultra-high density scanning-probe memories using re-writeable phase-change media

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ABSTRACT

In this paper we report on the systematic design of re-writeable, ultra-high density, high data rate scanning probe memories using phase-change media. The re-writeability of phase-change media from the amorphous to the crystalline phase or vice versa is investigated using a parametric variation approach. This enables the design of an optimized re-writeable medium stack for the re-writing of small, regular-shaped bits under low voltage/low power conditions.

Key words: scanning probe memories, phase-change memories, re-writeable memories

1. INTRODUCTION

Data storage density requirements continue to grow along with the need for decreasing power consumption. Recent advances in data storage and memory technologies has led to alternative, scanning probe-based phase-change memories[1]. In such applications, a particular attraction of phase-change materials is their re-writeability, since the basic storage mechanism of switching between amorphous and crystalline phases is inherently reversible. Re-writeability being the most attractive feature of current mainstream mass-storage technologies, it is important to understand the design issues related to re-writeability of probe-based phase-change memories. In this paper we address these design issues using a comprehensive (pseudo-3D) computational (COMSOL Multiphysics^{TM}) model for the electrical, thermal and phase-transformation processes, simultaneously solving the (time-resolved) Laplace equation, the heat conduction equation and the JMAK (Johnson-Mehl-Avrami-Kolmogorov) equation [1]. The model incorporates realistic material properties and critical temperatures.

2. SIMULATIONS

Fig. 1 shows a detailed schematic of the re-writable probe storage architecture comprising the encapsulated PtSi tip[2] and the GeSbTe (GST) storage medium. The basic design requirements were the ability to achieve the requisite amorphization and crystallization tempertures in the GST layer while avoiding excessive temperatures in the capping layer, while at the same time using only a moderate tip-sample voltage and a pulse duration suitable for high data rates (> 1Mbit/s/tip). Points A to D in fig. 1 are the locations at which maximum or minimum temperatures are specified in order to design the stack for the writing of both amorphous and crystalline bits. For the writing of amorphous bits the temperature at points A (at the top of the GST layer and under the tip center), B (at the top of the GST layer and at the edge of the tip conductive region) and D_A (in the middle of the GST layer and under the tip center) should at least reach the melting temperature (~620˚C) so that, when coupled with appropriate cooling rates, this region will solidify into the amorphous phase. Simultaneously with this requirement it is necessary to avoid excessive temperatures anywhere in the stack. Here we choose a maximum temperature that should not be exceeded of 1000˚C due to stack reliability issues at high temperatures. To avoid thermal cross-talk affecting previously written bits, point C is kept at a maximum temperature requirement of 200˚C. For the writing of crystalline bits in this study, the minimum

temperature that should be reached at points A and B in Fig. 1 is taken to be 300^0C. Temperature point D_C (at the bottom of the GST layer and directly under the tip center) is chosen to be a minimum of 300^0C, to ensure that the crystallization occurs through the full thickness of the GST layer.

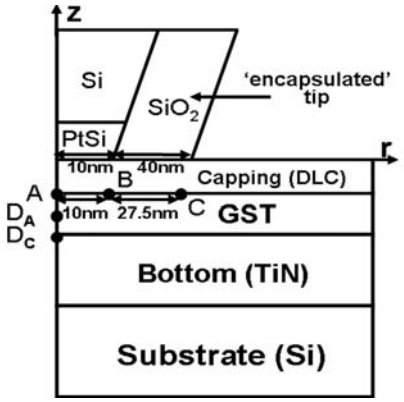

Figure 1: Schematic of the re-writeable probe storage architecture

	Tip probe		Capping	Recording	Bottom electrode	Substrate
	PtSi	SiO_2	C	GST (a/c)	TiN	Si
Thickness (nm)	N/A	N/A	2	5-25	40	150
Thermal conductivity ($Wm^{-1}K^{-1}$)	25	1.4	0.5-5	0.2/0.58	3 or 12	149
Electrical conductivity ($\Omega^{-1}m^{-1}$)	$3.3 \cdot 10^6$	$1 \cdot 10^{-12}$	10-100	See[1]	$5 \cdot 10^5$- $5 \cdot 10^6$	N/A
Density (Kgm^{-3})	12400	2200	2800	6150	5400	2330
Heat capacity ($JKg^{-1}K^{-1}$)	250	700	540	210	400	720

Table I: Characteristic parameters for the designed media stack

3. RESULTS & DISCUSSION

A parametric search for suitable values of the capping and underlayer properties (electrical and thermal conductivities, thickness etc) has been carried out using the aforementioned temperature and voltage/pulse duration requirements. The properties of a suitable stack design are given in Table 1. Using this stack design we have investigated four different routes for the provision of re-writeability in phase-change probe memories: (i) the writing of amorphous bits (in a crystalline starting phase) and their subsequent erasure by re-crystallization; (ii) the writing of crystalline bits (in an amorphous starting phase) and their erasure by re-amorphization; (iii) the writing of crystalline bits in a slow-growth material and erasure by re-amorphization; (iv) the writing of crystalline bits in patterned media (again with erasure by re-amorphization). In simulations we achieved success via all routes except (ii). In practice there are potential technical problems with all routes, as will be discussed.

4. CONCLUSIONS

In summary, a systematic design of practicable media suitable for re-writeable, ultra-high density (> 1Tbit/sq.in.) scanning probe phase-change memories has been presented. The basic design requirements were met by a Si/TiN/GST/DLC structure, with properly tailored electrical and thermal conductivities.

REFERENCES

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